REMARKS

The claims have been amended to make it clear that there are three distinct operations going on in the claim. First, the code addresses are broken into local memory sub-regions. Secondly, the global method lookup table is broken into smaller and distributed versions. Thirdly, one local memory sub-region is associated with one smaller and distributed version of the method lookup table.

According to the Examiner, the cited reference to Matula suggests modifying Shaylor to break up a lookup table. But, even if this is so, breaking up the lookup table is not commensurate with the scope of the claims here.

The claims here call for, not only breaking up the lookup table, but associating the lookup table with distinct memory sub-regions. In other words, the claims here call for breaking up a code address into regions of memory and, further, breaking up the table into corresponding regions. Simply teaching breaking up the table into parts does not reach all of the claimed elements.

Therefore, reconsideration is respectfully requested.

Respectfully submitted,

Date: September 8, 2008

Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.
1616 South Voss Road, Suite 750
Houston, TX 77057-2631
713/468-8880 [Phone]
713/468-8883 [Fax]

Attorneys for Intel Corporation